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Design and simulation of low dropout voltage regulator using 180nm technology

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***Abstract*---**Low Dropout (LDO) Voltage Regulators are the linear regulators which drives upon a very small differential voltage. The main components of the Low dropout voltage regulators are Error amplifier, Pass device, voltage reference source and Voltage divider network. The low dropout voltage regulator uses a variable input to give a steady, constantly controlled, low-noise DC output voltage. This is a linear voltage regulator that includes a small voltage drop among the input as well as the output that works even when the output voltage is extremely close to the input voltage. The Error amplifier circuit which is one of the components in Low dropout voltage regulator is designed in the standard 180nm CMOS technology, with supply voltage of 1.6V, the gain of the error amplifier is 74db, Band-

gap reference circuit is implemented to produce stable reference voltage which is independent of temperature variations. The bandgap reference voltage circuit gives the output voltage of 1.2V. The low dropout voltage regulator produces constant output voltage of 1.8V for the input voltage range 2.1V to 3.5V and it provides constant output voltage for load variations.

Keywords---LDO, voltage regulator, 180nm technology.

Introduction

Power management is one of several critical concerns in the design of those devices in order to meet product standards such as prolonged run time and reduced power consumption. Because of its unrivalled qualities such as low cost, tiny output ripple, and low power dissipation, the voltage regulator is one of the most widely used circuit components in this industry. Voltage regulators are essential components of all modern electronic devices and systems' power supply systems. Voltage regulators are power devices that maintain a constant and stable output voltage even with the input voltage variations or load variations. Various types of voltage regulators have been developed over time based on their design. The 'Low Drop-out Voltage Regulator,' frequently referred as the 'LDO,' is a voltage regulator with a low dropout voltage. Low-dropout regulators are defined by their ability to maintain regulation even when supply and load voltages change by a tiny amount. LDOs have shown to be effective instruments for achieving low power consumption and high-power efficiency in modern environment, as battery-powered devices pervade practically every part of life[1]. Due to the lack of a huge and expensive inductor, LDOs have a much lower footprint and greater overall value when compared to other types of inductors. LDOs are a simple and cost-effective way to regulate linear power. Low dropout voltage regulators serve two functions, the first of which is to reduce an incoming supply (input) voltage to the lower voltage required by the load. Another feature is the provision of a very low noise voltage source, even when noise is present. In comparison to switching regulators, LDOs are primarily employed because of their low-noise output voltage, low power consumption, small size, and low shutdown current, and inexpensive cost. They're ideal for noise-sensitive, high-frequency applications because of the clean voltage they provide. The pass element (pass transistor), error amplifier, and BGR circuit (reference voltage source) are the three basic components of an LDO.

Block diagram of low dropout voltage regulator (LDO)

Fig 1: depicts the basic LDO (Low Drop-out) voltage regulator topology. It consists of the (EA) Error Amplifier, two feedback resistors or voltage divider block, load, reference source voltage or the band gap reference circuit and pass transistor[2][3]. The dropout voltage which is the difference between minimum input voltage and output voltage, transient response, line regulation, efficiency, load regulation, power consumption, power supply rejection, and quiescent current can all be used to verify the performance of an LDO voltage regulator. The Pass transistor (pass element) works in the linear region to reduce the incoming

supply voltage down to the required output voltage and also supplies the incoming current to the load. Error amplifier (EA) sense the resulting output voltage and compares it with the reference voltage given by the reference voltage source, here the BGR (Band-gap Reference circuit) is the reference voltage source, and the BGR circuit is used whenever temperature independent reference voltage is required[5]

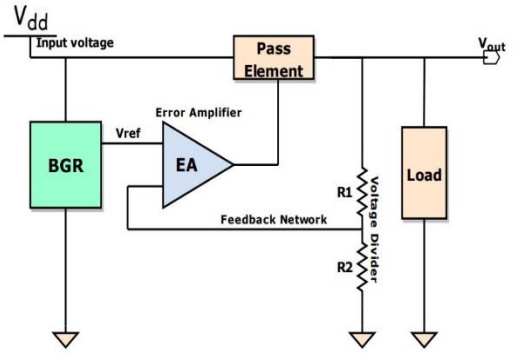

Fig 1: Block Diagram of Conventional LDO

Design of low dropout voltage regulator(ldo)

An error amplifier used in the proposed LDO structure is a two-stage CMOS operational amplifier (op-Amp). An op-amp is a circuit which is DC-coupled and high-gain electronic voltage amplifier with the differential inputs and having a single-ended output. Operational amplifiers typically have a very high gain, which causes the closed loop gain to become independent of the high gain of the op-amp when negative feedback is provided to such amplifiers[6]. The op-amps are designed with a large enough gain to provide proper negative feedback; the larger the gain, the more efficient the negative feedback op-amp will be. When negative feedback is used, stability, gain, and bandwidth depend less on internal circuitry and temperature coefficients[7][8].

Table 1: Design specifications of error Amplifier

Parameter	Values
A_{dc} Gain	>60db
GBW	35MHz
Slew Rate	$10V/\mu s$
ICMR+	1.6V
ICMR-	0.8V
V_{DD}	1.8V
I_{bias}	$20\mu A$
μNc_{ox}	300μ
$\mu pCox$	60μ

V_{TH3}	0.46V
V_{TH1}	0.41V
V_{dsat}	164Mv
gm_6	1.758m
gm_4	49.9μ
C_L	2Pf

It is assumed that all transistors are in saturation because in-order to work as an amplifier the above condition is required. The design begins by choosing a device length to be used throughout the Op-amp circuit.

Table 2: Aspect ratios(W/L) Ratios of error amplifier

Transistors	Aspect Ratio(W/L)
PM0	5.2
PM2	5.2
NM1	12.8
NM3	12.8
NM2	1.9
NM4	1.9
NM0	34.9
PM1	183.2

The two stage CMOS Operational Amplifier is used as an (EA) Error Amplifier of the LDO voltage regulator, since the two stage CMOS Operational Amplifier has a high input impedance and a low output impedance, in the proposed model the output of the 2-stage operational amplifier is connected to the differential amplifier of the fast and slow loops. The fast loop directly controls the gate of the pass element. Its purpose is to reduce spikes in the output voltage Vout induced by a change in the load. The amplitude of the voltage spikes and their recovery time have an impact on the regulator's overall performance. The slow loop's job is to maintain the DC output level by controlling the gate voltage of transistors. The slow loop is meant to have a low quiescent current and hence utilize less power. The circuit diagram of Error amplifier as shown below[9][10].

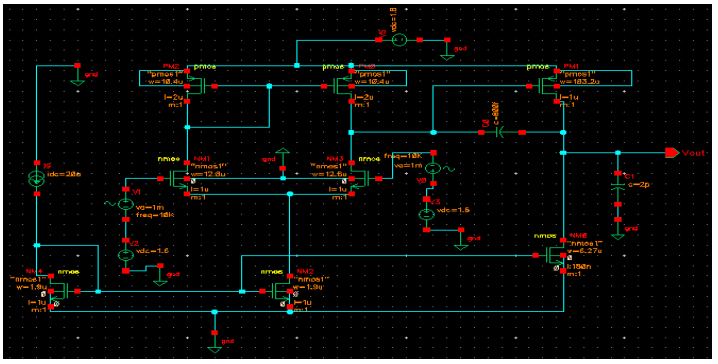

Fig 2: Circuit diagram of Error Amplifier

The function of a Band-gap reference voltage generator is to generally provide a stable reference voltage that is independent of the supply voltage and the temperature variation from its operation or from its surroundings. When we need a reference voltage which is independent of temperature, to compare it with another voltage which is dependent of temperature we use the BGR circuit. Generally, a band-gap voltage reference offers a great quality reference voltage at about 1.2V. Fig 3 shows the band-gap reference circuit along with a start-up circuit. Principle Operation of BGR circuit: Bandgap Reference Circuit provides the reference voltage (Vref) without being affected by the temperature (independent of Temperature variations)[11][12]. Temperature autonomy can be acquired by consolidating two peculiarities which are having opposite temperature coefficients. Thus, reference voltage of Bandgap Reference Circuit is the addition of negative temperature coefficient voltage and positive temperature coefficient voltage. In order word, Band-gap Reference Circuit consists of Proportional to Absolute Temperature (PTAT) and complementary to absolute temperature circuits (CTAT) that can compensate each other to give a constant voltage ideally regardless how the temperature changed[13][14]. The start-up circuit is used to pump the current to the BGR circuit and it will be disconnected automatically after pumping the current. Band-gap reference circuit provides a stable reference voltage that is independent of the supply voltage and the temperature variation. The circuit diagram of band gap reference circuit as shown below[15-18].

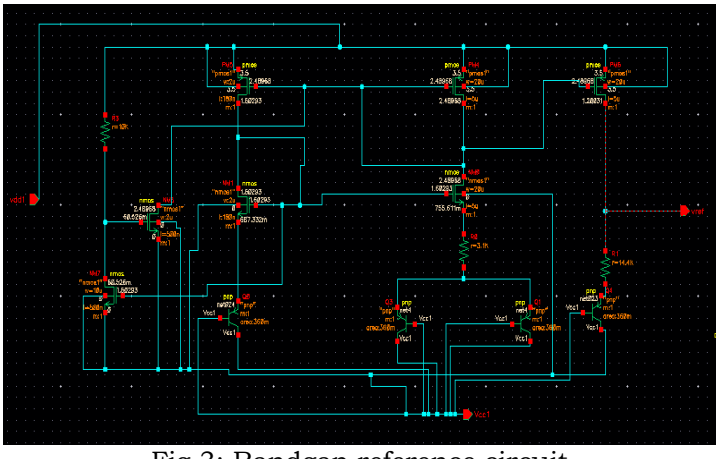

Fig 3: Bandgap reference circuit

The big PMOSFET having width 2m and length of 40u is used, In PMOS, the input is given to gate and the output is taken at the drain, the error amplifier will be having the Common-source configuration. Therefore, there will be phase inversion, hence the negative feedback loop/network will be given to the positive input of the Error amplifier. The loop gain of the PMOS pass element is more than the NMOS pass element. Hence for the design we have used the PMOS pass element instead of NMOS pass element and the resistors 100K and 200K as the voltage dividers, The Voltage divider consists of 2 resistors which are connected in series. It is used to provide different voltage levels from a single or common source of voltage, since the resistors are in series the voltage will not be same, but the current remains same in all components [19-23].

The following parameter used to design LDO:
Vref=1.2V
The LDO's output voltage is given as: Vout =V_{R2} + V_{R1}
R1=Voltage across resistor R1
R2= Voltage across resistor R2
The voltage across resister R2 will be same as Vref= 1.2V
The current through resistor R2 is I= V_{R2}/R2
I=1.2/200*10^3 = 6A
The voltage across resister R1 will be V_{R1}=I*R
Since the resistor are connected in series the current will be same through both the resistors,
Therefore V_{R1}=I*R = (1.2/200K)*100K
V_{R1}=0.6V
Vout =V_{R2} + V_{R1}=1.2V +0.6V =1.8V

Hence, we get the constant output voltage of 1.8V.

Table 3: Design specifications of the LDO circuit

Parameters	Value
Technology	180nm
Supply Voltage Range(V)	2.1-3.5
Reference Voltage(V)	1.2V
Output Voltage(V)	1.8V
R1	100K ohms
R2	200K ohms
PMOS Pass Element Width	2m
PMOS Pass Element Length	40μ

The low dropout voltage regulator as shown below

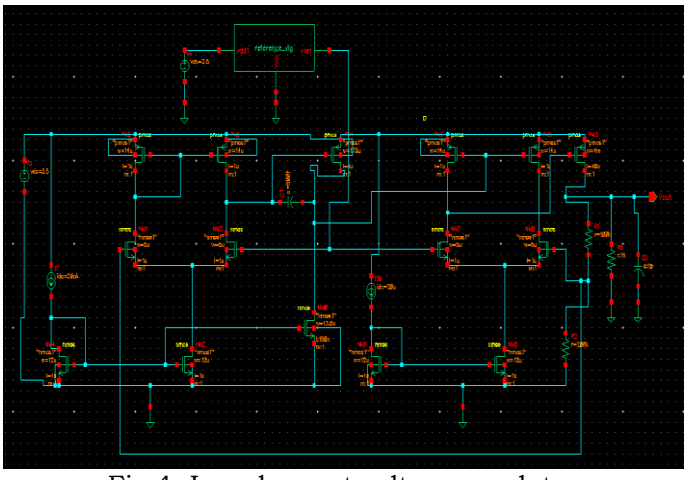

Fig 4: Low dropout voltage regulator

Results and Analysis

The dc analysis of the LDO as shown in Fig 5. The graph shows that the LDO operates from the range of 2.1V to 3.5V with a constant output voltage of 1.8V. Here we can see that the Vout will become constant after 2.1V of the input voltage and the Vout will decrease if the input voltage is less than 2.1V, we call this region from 0V to 2.1V as the drop-out region and the region from 2.1V to 3.5V we call it as the regulation region. Since the minimum input voltage for the LDO to operate is 2.1V and the output we are getting is 1.8V, we can calculate the drop-out voltage of the proposed LDO. 300mV is the Drop-out voltage. Here the drop-out voltage is the differential input to output voltage.

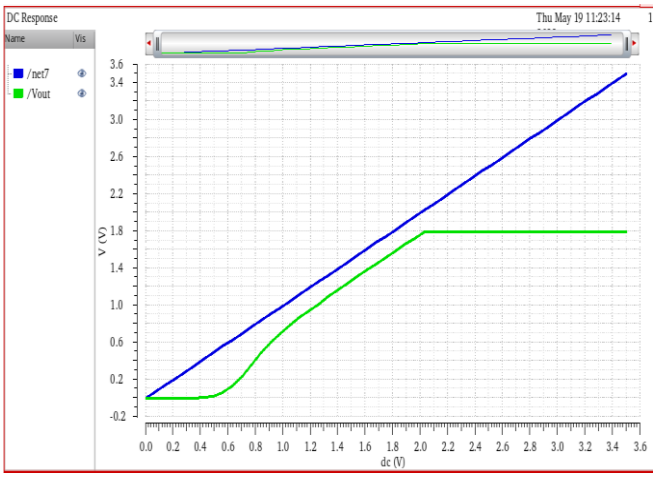

Fig 5: DC Analysis of LDO

Fig 6. Shows the transient response for the LDO from the graph we can see that the LDO regulates 1.8V output voltage for input voltage of 2.1V, with reference voltage Vref at 1.2V.

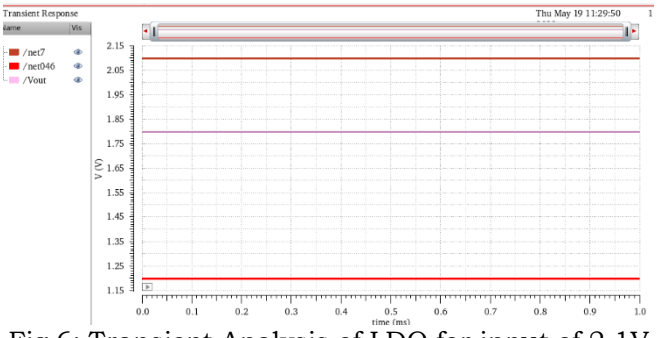

Fig 6: Transient Analysis of LDO for input of 2.1V

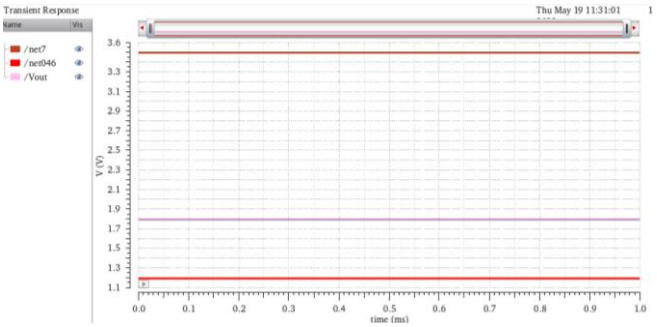

Fig 7: Transient Analysis of LDO for input of 3.5V

Fig 7 shows the transient response for the LDOs from the graph we can that the LDO regulates 1.8V output voltage for input voltage of 3.5V, with reference voltage Vref at 1.2V. From the Fig 7 and Fig 8 we can see that we output voltage will remain constant even though the input is 2.1V and 3.5V, while the reference voltage is 1.2V.

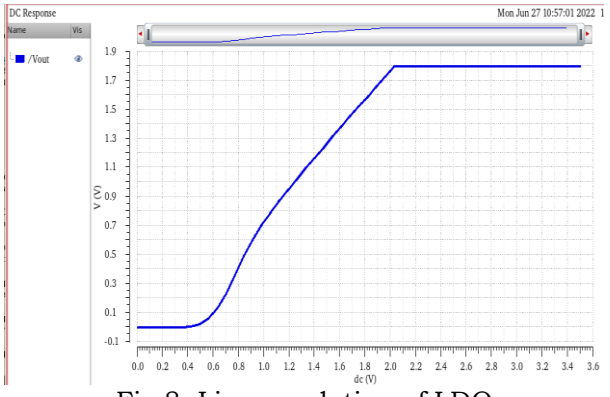

Fig 8: Line regulation of LDO

The Fig 9 shows the graph of output voltage with respect to the input voltage. Line regulation is the ability of the LDO to maintain specified constant output voltage with varying input voltage. Here we can see that the Vout (Output Voltage) will become constant after 2.1V of the input voltage.

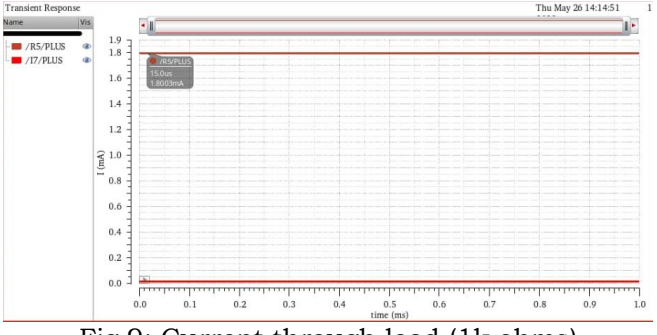

Fig 9: Current through load (1k ohms)

Fig 10. shows that the LDO is giving an output current of 1.8003mA through load of 1k ohm load.

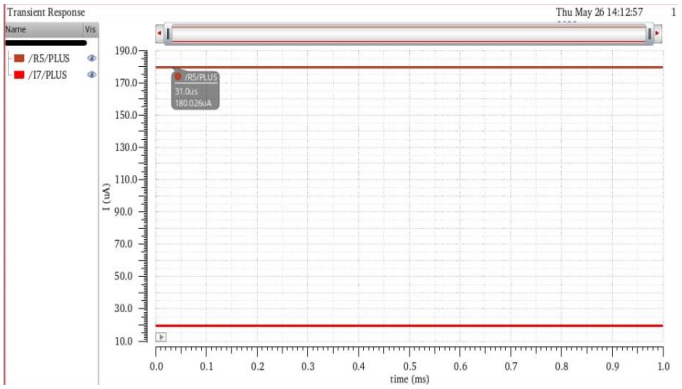

Fig 10: Current through load (10k ohms)

Fig 11 shows the current (mA) vs voltage (V) plot of the LDO when the output load resistor of 1K ohms is used, here we can observe that the current will exponentially increases along with the voltage and becomes constant after 2.1V.

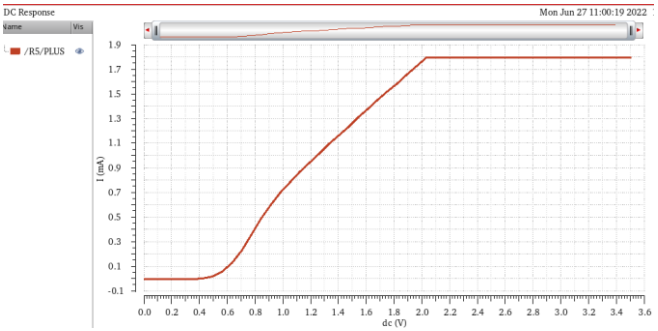

Fig 11: Current vs Voltage plot

The circuit produces constant output voltage of 1.8Volts with input voltage range 2.1V to 3.5V input current 20uA and reference voltage 1.2V, as shown in Table 4.

Table 4: LDO voltage regulator's performance

Parameter	Specification
Architecture	LDO voltage regulator
Technology	180nm
Input Voltage Range	2.1V to 3.5V
Input current	20uA
Output Voltage	1.8V
Drop-out Voltage	300mV
Band-gab reference voltage	1.2V
PSRR	-4.2db @1KHz
Power dissipation	9.75m Watt

Conclusion and future work

The proposed circuit has been simulated using 180nm technology in Cadence software and the simulation results have been analyzed. The proposed circuit provides a constant output voltage of 1.8V for the input voltage range of 2.1 to 3.5V with input current 20uA and reference voltage 1.2V. The Drop-out Voltage is 300mV and the Power dissipation of the LDO is 9.75mWatt. According to the continuous survey, the supply voltage range and foundry of the technology are both continuously decreasing as technology advances. Reduced technology allows for decreased power usage. Depending on the control signals, we can develop a low power, LDO that can produce a range of output voltages.

At the frequency of unity gain, the PSR of the LDO is high. A high pass filter can be inserted to further . The addition of this block would enhance PSR at the necessary high frequency without impairing low frequency PSR characteristics. The LDO's settling time is a few microseconds or less. This is impacted on by the loop's low GBW. This can be made better by increasing the LDO's GBW. However, this has an impact on stability or can be achieved with more power.

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