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Design of efficient DSP operation with 16x16 RMAC unit using cadence tool

Mrs. Leo Pauline
Assistant Professor, Electronics and Communication Engineering, Vel tech Multitech Dr. Rangarajan & Dr. Sagunthala Engineering College, Avadi-600062, Tamilnadu, India
Email: sleopauline@veltechmultitech.org

U. Megovia,
UG student, Department of ECE, Vel tech Multitech Dr. Rangarajan & Dr. Sagunthala Engineering college, Avadi-600062, Tamilnadu, India
Email: connect2megovia@gmail.com

C. Selvapriya
UG student, Department of ECE, Vel tech Multitech Dr. Rangarajan & Dr. Sagunthala Engineering college, Avadi-600062, Tamilnadu, India
Email: selvapriyac01@gmail.com

P. Gowmari
UG student, Department of ECE, Vel tech Multitech Dr. Rangarajan & Dr. Sagunthala Engineering college, Avadi-600062, Tamilnadu, India
Email: gowmarirk2000@gmail.com

***Abstract*---**Reversible multiplier and accumulator (RMAC) are the essential operation using in DSP application where DSP processor requires high performance with different application.so the speed of operation is increased only by, implementing and designing 16x16 RMAC. Since the power consumption and heat is high in MAC. It can only be reduced by using an RMAC and chips like FPGA get increases. Whereas three fetch decode-execute cycle is needed in MAC for simulation of result.so time delay and high quantum cost should be contained in circuit. Though single fetch-decode execute cycle is more enough to RMAC for simulation of result. Time delay were not required and quantum cost is low for the circuit. For long circuits using normal gates dissipates more heat. The operations performed by using reversible gates do not dissipate heat energy because the circuit reaches the input as well as output. In this reversible MAC, the gates, adder is reversible. Accumulator uses Fredkin gates. If single bit of information is lost, it diss-appear (kTln2) joules of heat energy for irreversible circuit. No more information mapping is lost in reversible

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***Corresponding author**: Pauline, L.; Email: sleopauline@veltechmultitech.org*
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circuits between input and output. It deals with VLSI design and FPGA technology. The proposed RMAC has 16-bit reversible multiplier, 32-bit reversible adder and 32-bit reversible accumulator. When additions and multiplications are performed in DSP operation, discrete-Fourier transform (DFT) computation is used. To minimize the consumption of power DFT computation is implemented by Verilog hardware description language (VHDL). The technology used in this project is application -specific integrated circuit (ASIC). Main applications of this project are digital signal processors, image processing and one- one mapping. For 16-bit multiplier and accumulator unit, the parameters like garbage output (GO) Reversible gates, Quantum cost (QC), constant input (CI) are computed and analysed. Whereas in 16-bit RMAC of DSP operation, it performs multiplication in reversible and addition. With reversible gates, movement of the signal (shifting) and accumulator is performed.

***Keywords*---**MAC, RMAC, Verilog Hardware description language (VHDL), Reversible gates.

Introduction

According to the research of Landauer's, using irreversible logic, in order to erase a bit, heat transfer of KTln2 joules is required [1]. In normal gates the output response. For each bit response it dissipates heat. Hence the large circuits using reversible gates it does not dissipate heat energy because the circuit reaches the input as well as output. Hence input to output mapping is existed in reversible gates [2],[11]. In reversible circuits, parameters like quantum cost (QC), Garbage output (GO), constant input (CI) and gate count (GC) are included for fixing the complexity, performance in the circuits. The circuit is designed based on four parameters. For processing high digital system, all DSP processor use MAC [12]. The MAC is useful in algorithms, Integrating the Multiplier and accumulator into arithmetic unit to increase the speed of digital signal processor. The paper is designed in domain of VLSI (very large -scale Integration) and technology used in this paper is FPGA (Field programmable gate array) [3],[4]. Very large-scale integration (VLSI), is the mechanism of producing integrated circuit. In this process thousands of transistors are merged into a single chip. Very Large-Scale Integration was started during 1970s when technologies like communication and semiconductor were being evolved. The microprocessor which is used in this technology is a device which disclose in VLSI. Most of the integrated circuits has a restricted set of tasks they could perform. The electronic circuit includes RAM, ROM, CPU and glue logic [2]. In VLSI all these above combines to make in a single chip. A sensational development was found in the electronics industry in the last ten years. This is largely due to expeditious headway in applications of system design and large -scale integration industry. As the emergence of very large-scale integration, a very fast rising of many numbers of applications of integrated circuits such as controls, high performance computing, image and video processing, telecommunications were arose. The present advanced technology for instance higher resolution, cellular communication and low bit rate video gives the customers a sensational amount of portability, processing power and uses.

Through much important intimation of system and VLSI design, this vogue was expected to develop quickly [1]. The Field Programmable Gate Array (FPGA) consist of ten thousand or greater than one million logic gates programmable linkages. These are available for end-users to do the given task at ease. A classic model FGPA chip is represented in the below figure. This includes I/O blocks which are mapped out and numbered as stated by the function [15]. There are Configurable Logic Block (CLB's) in logic level construction for every module. The logic operation was performed to the assigned module. Using horizontal routing channels, vertical routing channels and programmable multiplexers (PSM), the linkage between I/O blocks and CLB are made. The convolution of FPGA determines only the CLB it contains. VHDL or any other Hardware descriptive language sketches the performance of CLB's and PSM. These are fixed on the chip and linked with every routing channel [5],[6],[7].

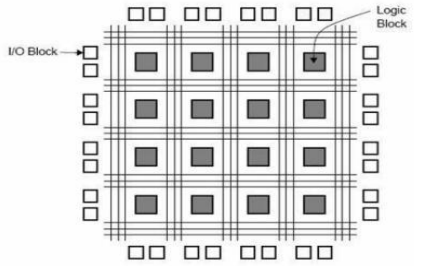

Fig. .1 Linkage between routing and CLB

In normal mac unit uses irreversible gates.This normal MAC which multiplies,adds and accumulates. Hence for lare circuits it will take more times and also generate more heat. Hence RMAC is designed to avoid this problem.

Existing System

MAC consists of the most important system in many DSP application. MAC is the process of multiplication and accumulation. In DSP systems, MAC is used only when the system performance is high. The main function of MAC unit gives filtering in high speed and for DSP application it gives other processing characteristics. A large quantum of digital data is most required for fast process [12]. To perform the operation in digital signal processing, MAC performs multiplication and accumulation. Two n bits of inputs are given to a Multiplier and the product of two n-bits are added to an adder as 2n bits whereas carry will add 1-bits to an 2n-bits and it get into an accumulator and 2n+1. The final output will be executed with an addition of carry so it takes more time for simulation of result. Data are used high in MAC and power consumed rapidly. Hence, the system might be slower to process. In an existing system, the performance of MAC is explained in detail [13],[15].

Operation of mac

In digital signal processing application and in various other application, one of the essential key-operation is said to be MAC operation. In this paper, 32bit RMAC unit is designed [15],[8]. The register used for parallel in parallel out is said to be

accumulator register. Since, No. of bits are huge. The input and output of the parallel in parallel out (PIPO) registers are used to take in the form of parallel. If the one input to carry is supposed to save the adder then the accumulator register output is removed [11].

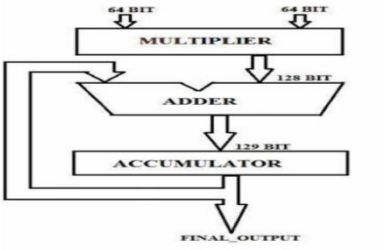

Fig. 2. General framework of MAC

Multiplier

It is designed by modifying Radix 2 both multipliers. The arrival of one chip multiplier gives the result for DSP function in very large-scale integrated chip. Speed, Accuracy, Dynamic Range is the features of multiplier. The product of two inputs were said to be multiplier [4].

Multipliers in parallel

A multiplication done in parallel form is said to be multiplier in parallel. X and Y be a multiplier of two numbers. X is using m bits and given as (Xm-1 Xm-2....X1X0) and Y is using n-bits and is given as (Yn-1 Yn-2 .....Y1Y0). The below calculation is the result of parallel multiplier.

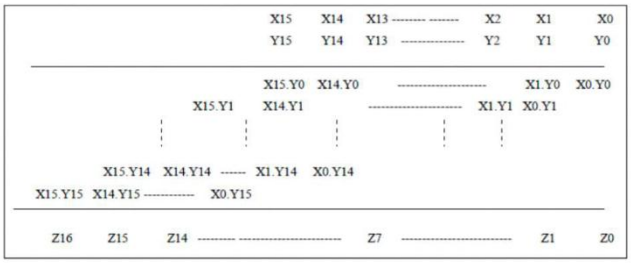

Fig.3. Parallel Multiplier

Adders
Half Adder Circuit

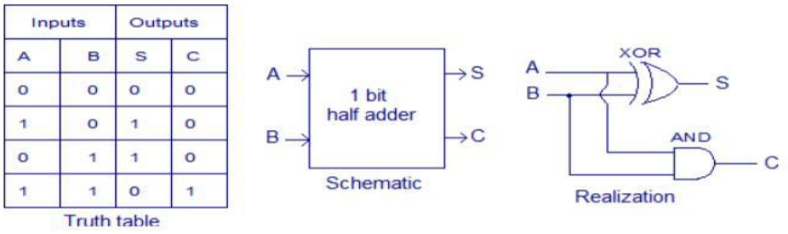

Fig.4. Truth table and half adder circuit

A sum bit (S) and carry bit(C) is executed when half order is combined to add two numbers. The sum bit (S) will be X-OR of two Numbers and the carry bit(C) will be AND of two Numbers. Using single X-OR and single AND gate, half adder is formed elaborately [7],[13]. In MAC unit, half adder take carry if it is given in input. Though the input is given in the half adder will be added to the accumulator and the consumption of power remains higher in using Half adders.

Full Adder

It is a digital circuit that performs addition. It adds three one bit of binary numbers,2 operands and a carry. The output will be 2 numbers, Sum and carry bit. It is opposite with a half adder, that adds two binary digits. It consists of three inputs and two outputs. The full adder is used in MAC that will increase the power consumption by giving three inputs and two outputs will be executed. It will slow down the system operation and the power consumption get higher in MAC unit [7],[13].

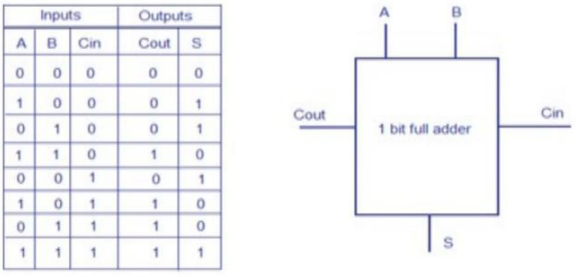

Fig. 5.1bit full adder truth table and schematic diagram

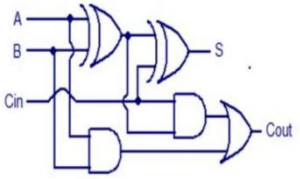

Fig. 6. Full Adder Circuit

Ripple carry or parallel adder circuit

The n number of full adders cascaded combinedly then the ripple carry adder is formed. At simple logic gates, it will add combinedly two binary numbers. Ripple carry adder consists of full adder in chain, with the output from each full adder in chain [9],[10]. The total propagation time is equal to the propagation delay of a typical gate, then the number of gates levels in the circuit. In ripple carry adder more amount of time is created to execute an approximate output. From the figure given below, with inputs '0' and output '1' consider a NOT gate. Now the output of the NOT gate to be executed as '0' when the input gates after the logic '1' is said to be propagation delay [14].

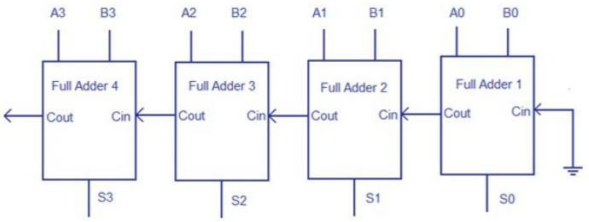

Fig.7. 4-Bit Ripple carry or parallel adder circuit

The delay in the propagation of carry is said to be carry propagation delay. In MAC operation, ripple carry adder will take much more time to give an exact output and the time taken will increases the consumption of power more-heavier. Then the data might also be used rapidly. A complexity in ripple carry adder with propagation delay can be done through carry look ahead adder.

Accumulator

Accumulator is a device or register which can contain short-term arithmetic and logic data of CPU in a computer. When the sum is found, it is put down in main memory or any other register [11]. Accumulators are used in wide range of non-calculating operations and uses. Those are electrical engineering that is a refillable battery which can store the energy or ultra-capacitor, hydromechanical or hydraulics (device which can store mechanical energy), trading market which is an agreement or contract, or a wager which is to place a bet [4].

Flip-flops and registers

The NAND gate is used with set reset or latch to control it in an easy manner. The set-reset will be constant, if the output of the NAND gate is 1 with enable 0. And Q values are similar to data with enable 1. When enable is 1, the changes made in data also changes the output of Q [7]. When the enable is 0, the output of Q will be the previous value of D and Q' is opposite.

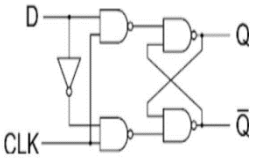

Fig.8. D-Flip flop

The locked first output is shown by the second flipflop output. Even the second set reset is parallel state, the output that contains data are not change since the set reset of first is closed [4].

If enable is low, the flipflop of second set-reset will be closed first. Then the first set reset is in parallel state the output that contains data are also not change because the flipflop of second is closed now. If the enable input is from low to high, then a new data can be stored in the circuit. The two flipflops are opened by a box and shown in a single symbol [6].

Universal shift register of parallel in parallel out

The concept of parallel in and parallel out universal shift register is that the inputs are taken in parallel form and the output are also shown in parallel. In universal shift register, the shift of both right and left are in form of parallel. Using the shift register, the storage and memory are more obtained to save the data. The universal shift register is used to save all kind of data, if the data might also larger can also save in the shift register [3],[11].

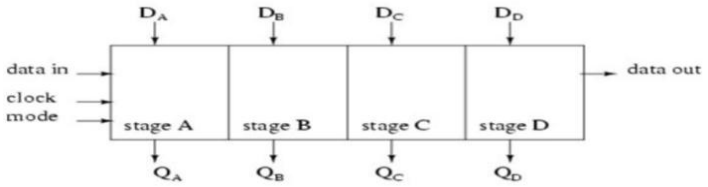

Fig. 9. PIPO Shift Register

Proposed Mac Design

Reversible multiplier

Reversible adders is used to multiply two binary numbers is said to be reversible multiplier. This will reduce the power dissipation, reducing number of reversible gates, delay and quantum cost. The multiplication is a set of partial products generation and multi operand addition.

Generation of partial product

The partial product is generated by AND in binary logic. It is of 256 partial products in the term of Xi and Yi. The variation of 'i' varies from 0 to 15. Peres

gates and RAM gates are used here. Generation of 256 partial product is only by the 256 partial generation. Copying gates are used by RAM gates.

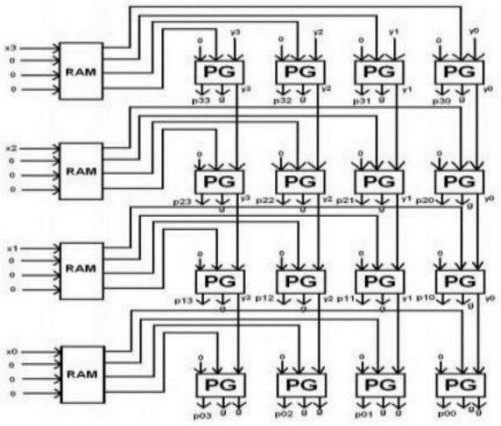

Fig.11: Proposed Reversible Partial Product Generation Circuit

Multi-operand addition

Partial product addition is performed by using PG and DPG gates. The fundamental cell for this multiplier is full adder. Two garbage outputs, three inputs and one static input from DPG is used by the full adder. In the place of half adder PG is placed as it has a garbage output, two inputs and one static input. The multiplier user here which is a reversible circuit contains four chunks. Each block contains sixteen DPG, eight PG, 32 PG. This is on behalf of partial product generation and eight spread out RAM gates. In the place of eight RAM 24 FGs are needed as the FG is applicated in copying circuit. Thus, the trash outputs and hardware difficulty are decreased by means of RAM gates.

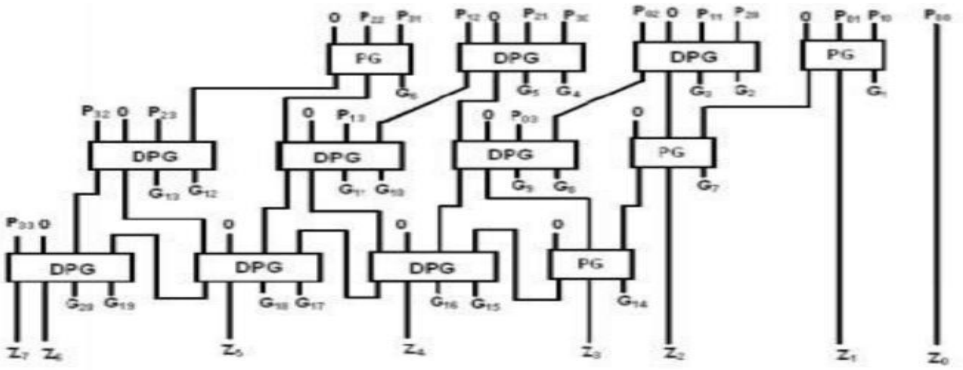

Fig.12. Reversible Multi Operand Addition Circuit

Reversible Adder
Reversible Half Adder/Subtractor

It is processed by using three reversible gates like one Peres gate and two Fredkin gate. The Peres gate contains 3*3 reversible gate that is of three inputs and outputs. The inputs are connected with an output. The Peres gate contain four quantum cost and gates like two V+, one V and one CNOT are also used in the Peres gate. The Fredkin gate also contain 3*3 reversible gate that has inputs of three and outputs of three. The inputs are connected to output same as like the Peres gate. The quantum cost is 5. Two patterns of rectangles which are similar to 2*2 Feynman gate is required. A multiplexer is processed by using the Fredkin gate g1 and g2 are garbage inputs.

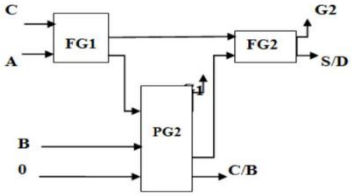

Fig.13. Reversible Half-adder

Reversible Full-Adder

It is processed by using four reversible gates like two Peres gate and two Fredkin gates. Where g1, g2, g3 are the garbage inputs. The double Peres gate contains 4*4 reversible gate. The four inputs are mapped to the four outputs. Six quantum costs are contained. It is opposite of a reversible half adder. The outputs s and c are sum and carry. The Peres gate and Fredkin gates are reversible gates. The reversible full adders are used to implement the operation rapidly with consumption of low power. Reversible gates are mapped together and it execute constant outputs with less delay time. The power consumption is also less at the time of process by using a reversible-gates. More density is required.

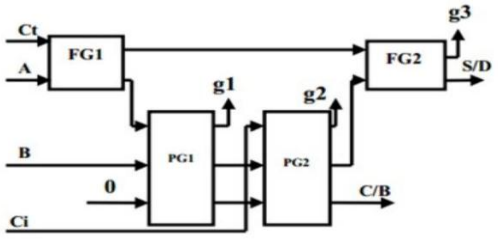

Fig.14: Reversible Full Adder

8-Bit reversible parllel binary adder

The reversible 8-bit parallel adder is constructed using the reversible half adder or subtractor and full adder is shown in below figure. The 8-bit addition and subtraction are varied using the central input. Carry and borrow is meant by C_B1 until C_B7. The binary 8-bit numbers are A0, A1, A2, A3, A4, A5, A6, A7

and B0, B1, B2, B3, B4, B5, B6, B7. This includes a half adder or subtractor. Here the half adder comes in initial level.

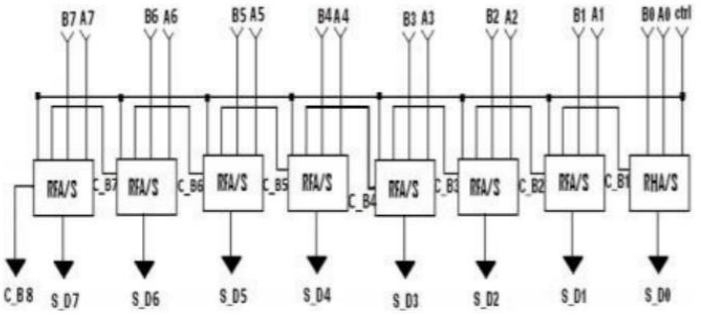

Fig.15. 8-bit reversible parallel binary Adder

Reversible accumulator

In a system processing the device is more expanded in an accumulator. Accumulator is said to be a register in which intermediate arithmetic and logic results are stored. To obtain the reversible accumulator it uses reversible register. An information bit is saved within a system with a set of flipflops that are combinedly connected. R-PIPO shifts register is used in reversible accumulator. It is obtained by reversible gates and the reversible delay flipflop is used here to pre-loop the carry from an adder.

Delay-Flipflop- Reversible

Flip flop consist of 2 constant states and 1-bit memory device. The expression of d-flipflop is D=Q n + 1. CLK+Q, here the CLK 1 can be charted on the Fredkin gate at ease.

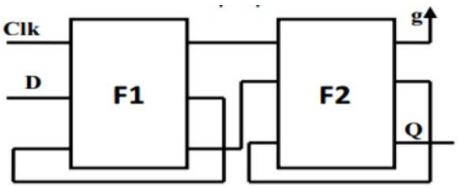

Fig.16: Reversible D-Latch

Reversible Eight -Bit Pipo Shift Register

Reversible D flipflop is used by the shift register. An 8 delay flipflop is used in 8-bit reversible PIPO shift register. Whereas 32 delay flipflop is used in 32-bit reversible PIPO shift register for 16x16 RMAC unit. This is very difficult to execute by using 16x16 RMAC unit. And it is implemented by using an 8bit PIPO shift register. The inputs are (D0, D1, D2, D3, D4, D5, D6, D7) and the inputs are (Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7). The inputs are parallel into the shift register same as well as the output are parallel to Q flipflops. The clock is used in each 8bits.

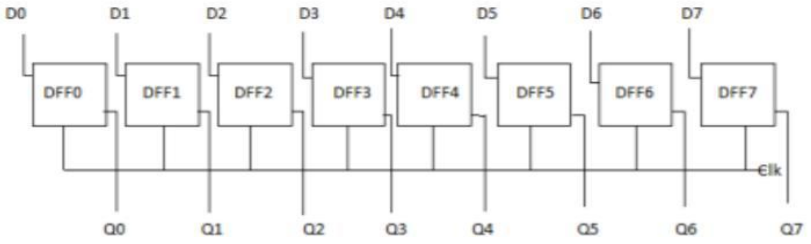

Fig.17: Reversible Eight-Bit PIPO Shift Register

R-Multiply Accumulate (MAC) Unit

The 16x16 R-MAC unit describes about 3-bit reversible MAC (RMAC) unit in the figure given below. RMAC unit performs to reduce the time delay by the processor to execute an exact output and the memory space were expanded in terms of using on-chips. These processes were operated by an RMAC as multiplication and accumulation combinedly to avoid unwanted problems and dumped process were also controlled by using RMAC. The introduced RMAC used in this paper is of 16bit reversible multiplier and 32bit reversible accumulator.

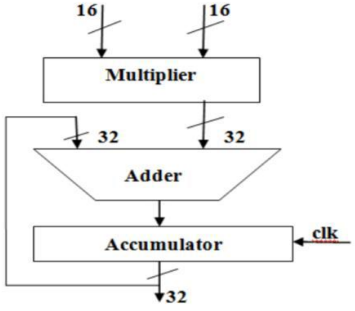

Fig.18. Reversible 16-bit Multiply-Accumulate unit

From the above diagram, the inputs of a reversible multiplier were multiplied and it was sent to an adder. The reversible multiplier was adder to the non-multiplied accumulated result, this has been done through adder.

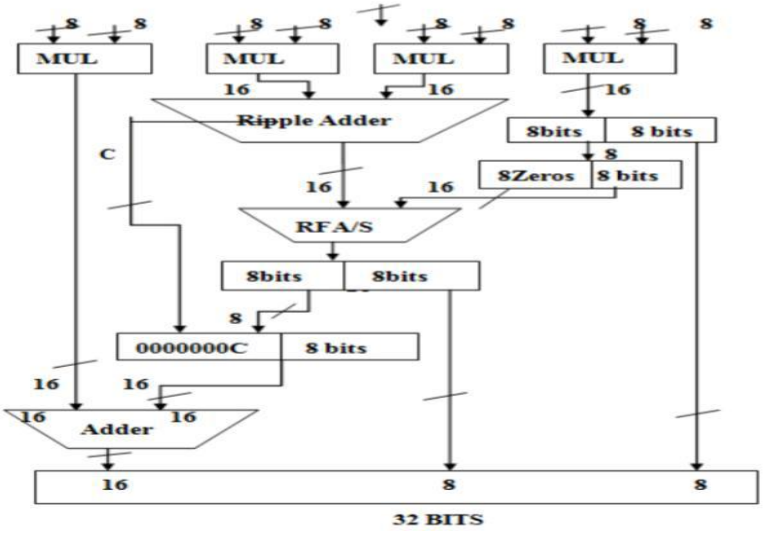

Fig.19: Reversible 16 x 16 Multiply and Accumulate unit block diagram

When a system performs addition and multiplication then discrete Fourier transform is used and that will used to reduce the consumption of power. RMAC introduced a Discrete Fourier-Transform computations.

Simulation Result

Simulation result is the output of the paper which shows low usage of power with an accurate output. This result will be useful for the next generation to analyze and understand the process. A detailed applications are also generated in this result.

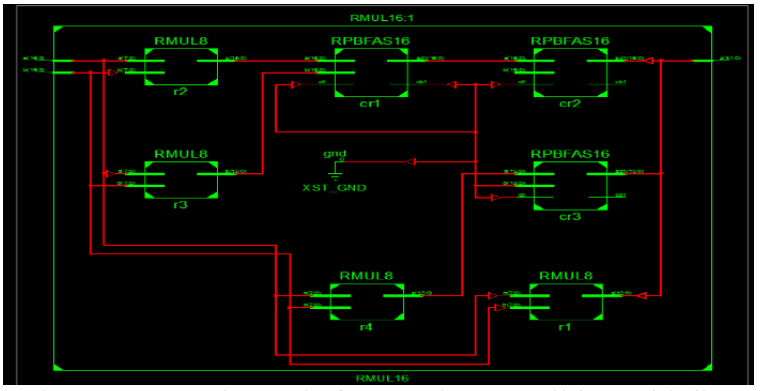

Fig. 20. RTL Schematic for 16 Bit Reversible Multiplier

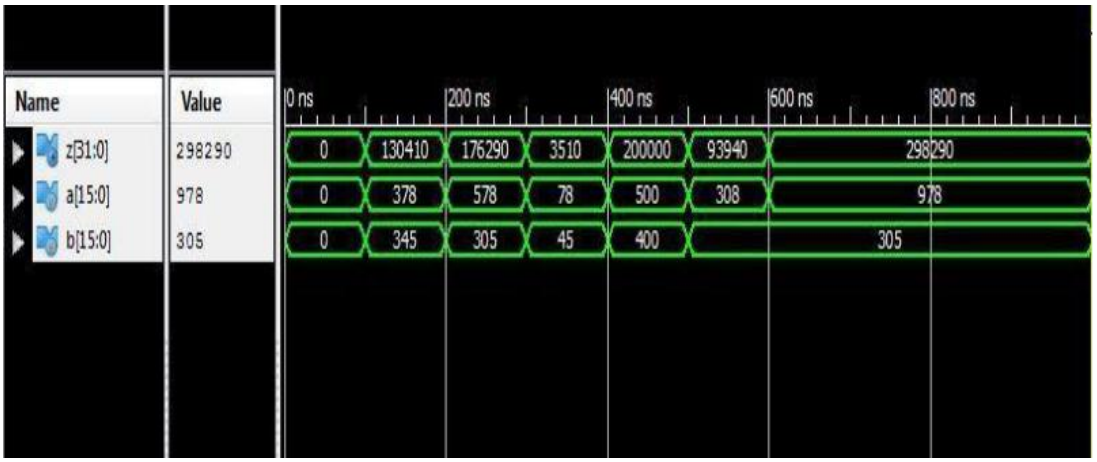

Fig. 21. Simulation Result for 16 Bit Reversible Multiplier

Table1
Performance analysis

Parameter	Power	Delay
Conventional MAC unit	363926.99(n W)	110.998ns
Reversible MAC unit	281869.6(n W)	95.725ns

The above table gives the performance analysis of the proposed system. From this we can conclude that comparing the conventional MAC unit, reversible MAC unit has low power consumption and it also have less delay comparatively.

Conclusion

In this paper, 16x16 RMAC is designed by a digital signal processing. The tools used in this project is cadence tools. A 16bit RMAC is designed by 8bit of reversible multiplier, 16-bit of both reversible adder and accumulator register. More number of reversible gates are used in this project to design the process of reducing the usage of power. Garbage output (GO), quantum cost, constant inputs (CI), Reversible gates are checked and verified for a 16-bit RMAC unit. And the parameters used in RMAC is less compared to the MAC operation. Hence, the power-consumption will be decreased in a certain amount of time with RMAC unit whereas in MAC, high usage of power is used in a system. This study evocatively expresses the 16 X 16 RMAC unit. This will help the future researchers to know more about RMAC operation and choosing a satisfying RMAC. This is applicated in the ASIC (Application Specific Integrated Circuit) and FPGA (Field Programmable Gate Array) for the purpose of signal processing. Relative study is due to the process of fabrication, performance of speed-voltage, low power consumption method, PPRT (Partial Product Reduction Tree), size or structure and number of clock cycles.

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