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Implementation of 12 bit R-2R DAC using cadence(90nm)

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***Abstract*---**An R-2R DAC utilizes less special esteem which is in contrast with to the binary weighed- input DAC. Continuous sampling and measuring of an analog signal occurs over time. This project depends on R-2R Ladder for investing Low power utilization, no dynamic chip and Low DNL. The DAC is executed in a virtuoso device on 90 Nanometer CMOS Technology. The two stages in our projects seems to be Operational Amplifier and R-2R Ladder Digital to analog converters enable transmission of analog signals over digital signal processing chips [1].Two stages are involved in the OP-Amp, the first one being a differential amplifier. We use this Differential Amplifier to obtain high gain and second stage namely Common Source Amplifier. It increases Gain that leaded from the first stage and increases it Output swing. In our project,R-2R DAC is implemented using CADENCE 90nm tool.

***Keywords*---**DAC, cadence, R-2R.

Introduction

An Digital to Analog Converter transforms computerized signals into standardized signals. Signals can be processed and stored digitally. A Digital to Analog Converter is playing a vital role in Digital Signal Processing [2].Changing the format of a signal can be done at any time. This is a device used to convert digital code into analog value. In modern technologies, less area is required, less expense is incurred, and computation takes less time. The remarkable growth of the electronics industry is largely a result of advances in large-scale integration technologies ICs can be used in a variety of applications including control, telecommunications, high-performance computing, and consumer electronics as a whole with the arrival of VLSI technology. We have met these demands with VLSI technology, which increases frequency while reducing delay. Researchers contend that dissipation and power consumption must always be taken into account at all stages of design Parameters. In this regard, it is deemed essential to consider power consumption and dissipation at all stages of design. Parameters such as circuit execution, power, and strength are specifically affected by the type of logic style used.

Proposed System

Easily designed for any number of bits, DAC uses only two values of resistors, output impedance of this DAC is fixed i.e. R, irrespective of a number of resistors[3].Depending on the logic style chosen for the circuit, parameters like execution, power, and strength will vary. Wireless devices, as well as hand-held devices and very fast processors, have driven the development of CMOS circuits. Innovation and technology scale the source voltages and transistor size to meet this requirement. As the number of transistors per chip increases, the interconnection density increases as well. When the interconnect density is high along with the clock frequency, the capacitive coupling of the circuit increases. Therefore, Again, when the supply voltage is scaled, which results in an increase in leakage current, logic failure and delays occur, Circuit performance must be preserved by scaling the threshold voltage.

Implementation Architecture

DAC Design

Our article focuses on the development of a 12-bit digital to analog converter. Figure 1 shows the implementation of the 12-bit R-2R DAC. Signal processing is used widely in applications like audio, controls, communication, and medical systems[4].DACs function by taking digital samples from a recorded signal and converting them into an electrical signal that can be played back. They do this by translating bits of data from digital files into an analog electrical signal at thousands of times per second, otherwise known as samples. A DAC outputs a wave that crosses all those points. However, because DACs aren't perfect, this can sometimes cause problems. There are several problems associated with high-frequency digital to analog converters when they operate at high frequencies, including jitter, reflection, narrow dynamic range, and limited bitrate. Converters

are classified based on the bandwidth and sampling criteria [6]. For this circuit, an operational amplifier and R-2R resistor network are used in figure 1.

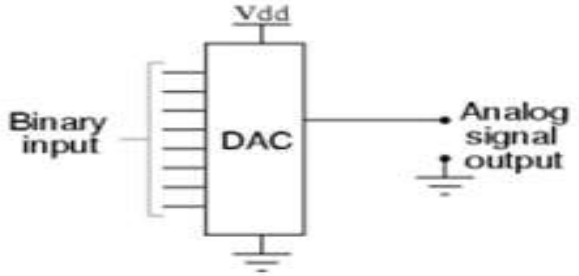

Figure:1 DAC diagram

Design of OP-Amplifier

It is used to perform mathematical operations on an input voltage. It will be having high gain and input impedance. With an OP-AMP, two terminals are needed, one for reversing phase, the other for maintaining phase, along with an output terminal. Two stage op-ampwith miller compensation capacitor (Cc) and nulling resistor (Rz) is used in this DAC design to provide stability for the output DAC signal. NMOS differential pair is used for first stage followed by PMOS common source amplifier[7].An op-amp is an amplifier having high gain and input impedance which is used to perform mathematical operations on an input voltage[8].Finally, the output is taken from transient, AC and DC analysis as shown in figure 2.Using operational amplifiers in mathematical computations, we can create linear, nonlinear and frequency dependent circuits with differential input and single-ended output.I n integrated circuits Op-amps are widely used because of their versatility. Different characteristics are taken into consideration in the trade-off curves, such as gain, phase margin, bandwidth, common mode rejection ratio, as well as power consumption.

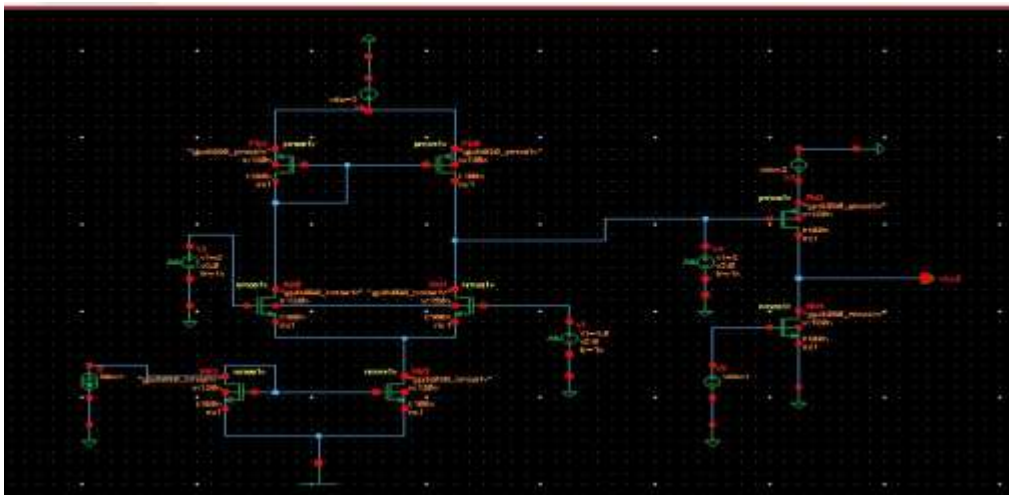

Figure: 2 OP-AMP block diagram

Characteristics features of OP-AMP

- Open loop Gain
- Open mode Gain
- Common mode rejection ration
- Slew rate
- Common mode voltage range
- Unity gain Bandwidth
- Total power dissipation

Design of Differential Amplifier

Op-amps are commonly used in integrated circuits because of their versatility. As well as gain, phase margin, bandwidth, and common mode rejection ratio, the trade-off curves are computed, as well as power consumption. An amplifier's capability to cancel voltages common to both inputs is indicated by its common-mode rejection ratio (CMRR), normally defined as the ratio between differential-mode gain and common-mode gain in Figure 3, the History of DA can be traced back to the vacuum tube age, with the first patient on it filed by Alen Blumlein in 1936. DA rejects common mode signals such as noise and amplifies differential signals as seen in Figure 3.Due to the configuration of their inputs, The output voltage of an operational amplifier will be proportional to the "Difference" between two voltage signals applied to one input terminal and another input terminal. Therefore, operational amplifiers are differential amplifiers. Unlike adders, which add or sum input voltages together, differential amplifiers produce much stronger signals by amplifying the voltage differences between two input voltages. This type of amplifier is commonly called a Differential Amplifier. As long as device characteristics in a pain of vacuum tubes or transistors remain the same, the DA comes from the notion of a bridge circuit using two vacuum tubes or transistors. One of the salient advantages of the DA is its tolerance to variations in device characteristics.

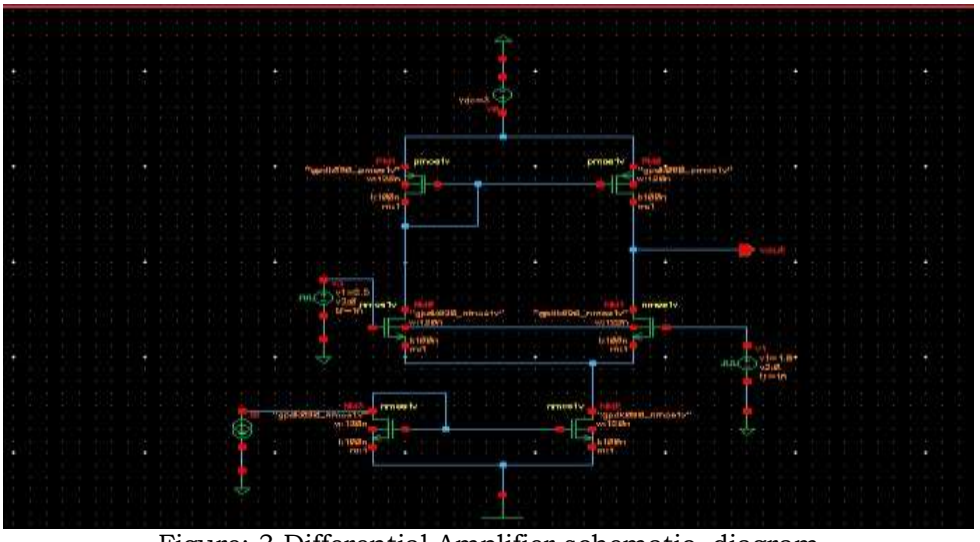

Figure: 3 Differential Amplifier schematic diagram

Design of common source amplifier

Current flowing through transistor can be calculated based on slew rate and capacitance [10]

$$slew\ rate\left(\frac{dv}{dt}\right)=\frac{I}{CL}$$

In the saturation region of M1 and M2, Vds>Vgs-Vt, as Vt is equal to 0.4v. The saturation region current expressed as

$$Ids=\frac{\mu C_{ox}W}{2L\left(V_d-V_S\right)^2}$$

$$g_m=\frac{\partial I_{ds}}{\partial V_{gs}}$$

$$Gain\ bandwidth=\frac{g_m}{2\pi fCl}$$

$$\frac{W}{L}=\frac{g_m^2}{2Ids\mu C_{ox}}$$

CS Amplifier

Common source structure is the basic of an amplifier[11].There are two stages in the OP-AMP design. The first stage is used to improve the gain and output swing of the differential amplifier. The second stage is used to improve the trans conductance amplifier or voltage amplifier. The diagram of the Common Source is given in the Figure4.However the gain depends on RC resistor. To have a large gain, RC must be large but large RC makes VD smaller hence MOSFET may clip into Triode region. So, instead of RC if we put a device which offers high resistance for small signal and low voltage drop for DC, we can achieve relatively large gain. We use a PMOS transistor in saturation region as an active load which offers high resistance for small signal and low voltage drop for DC.

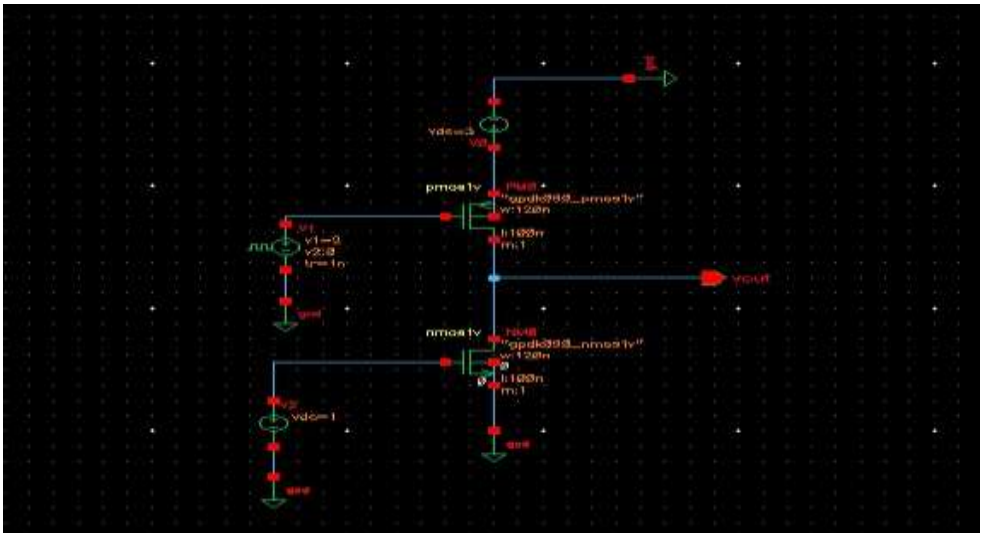

Figure: 4 Common Source amplifier

Applications of C/S Amplifier

The various application of Common source amplifier [11]

- cascade amplifiers and RF amplifier circuits.
- communication systems like TV and FM receivers.
- voltage-controlled devices in op-amps.
- Amplification of sensor signals.
- Low noise amplification of RF signals.

R-2R Architecture

For a weighted resistor D/A converter, R-2R ladder Digital converter provides a way to overcome the wide range of resistors in use. R-2R ladder Digital-analog converter allows current flowing through any input resister to encounter two possible paths. In the present paper a 12-bit R-2R ladder resistor DAC is implemented [12]. Neither path has a greater resistance than the other, so the incoming current is evenly split between the two directions. As part of the R-2R DAC, resistor ladders are designed by connecting resistors in series with R-value. Then, rungs of resistors are connected with 2R-value [13].Due to the half-current flowing backward it has no effect on the op amp's output voltage. However, the half that follows the ladder to the op amp affects the output voltage .In Figure 5, the incoming current is split evenly along the two paths due to the same total resistance along both paths.

Design of R-2R Ladder Amplifier

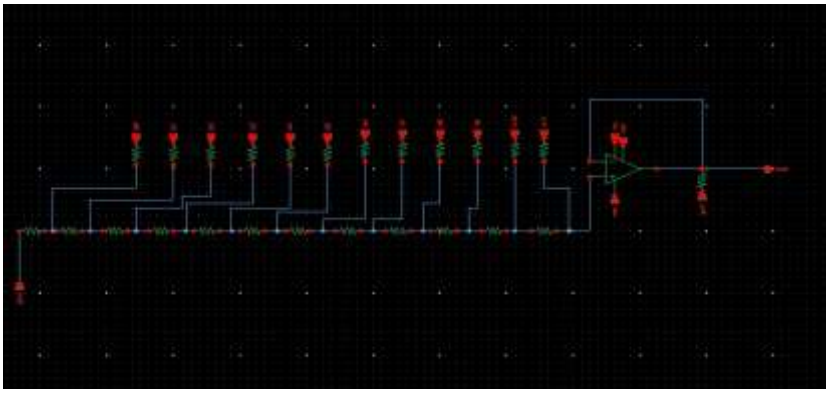

Figure: 5 R-2R DAC

The R-2R ladder resistor DAC is designed starting with two stages OP-AMP. So, it is necessary to design Op-amps with very low power consumption [14]. Starting at this power, and using supply voltage of 1.8V in 90nm n-well CMOS technology, the DAC is constructed .As the input transistors decide the gain of the op-amp, the value of total current flowing through them is calculated as well. Since a digital-to-analog converter offers 12-bit resolution, maximum current is passed through the input transistors for the system to be stable, the minimum op-amp gain is 2N+1, i.e. 42dB, and the phase margin is greater than 600.

Simulation Result

a. Differential Amplifier Result

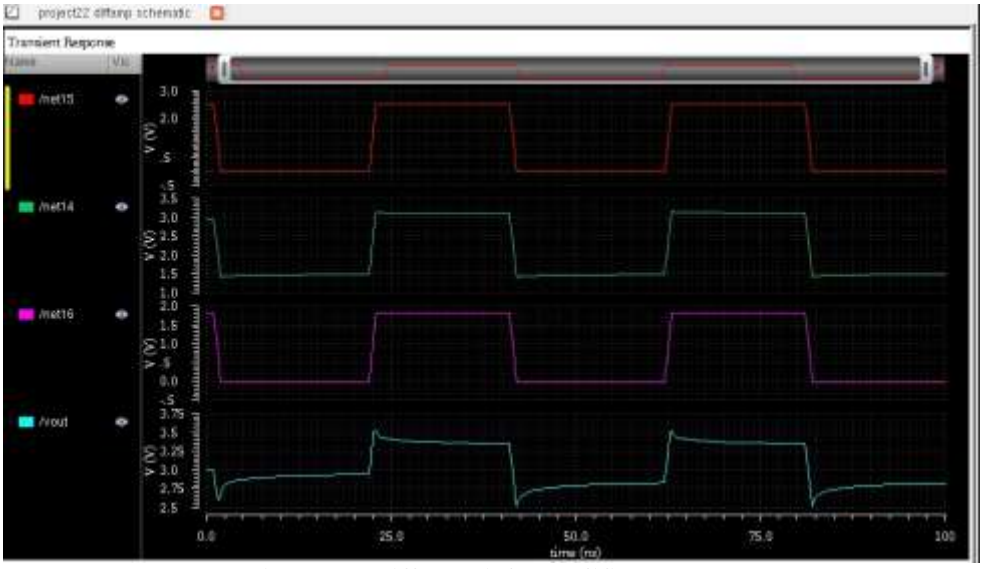

Figure: 6 Differential Amplifier output

b. Common Source Amplifier

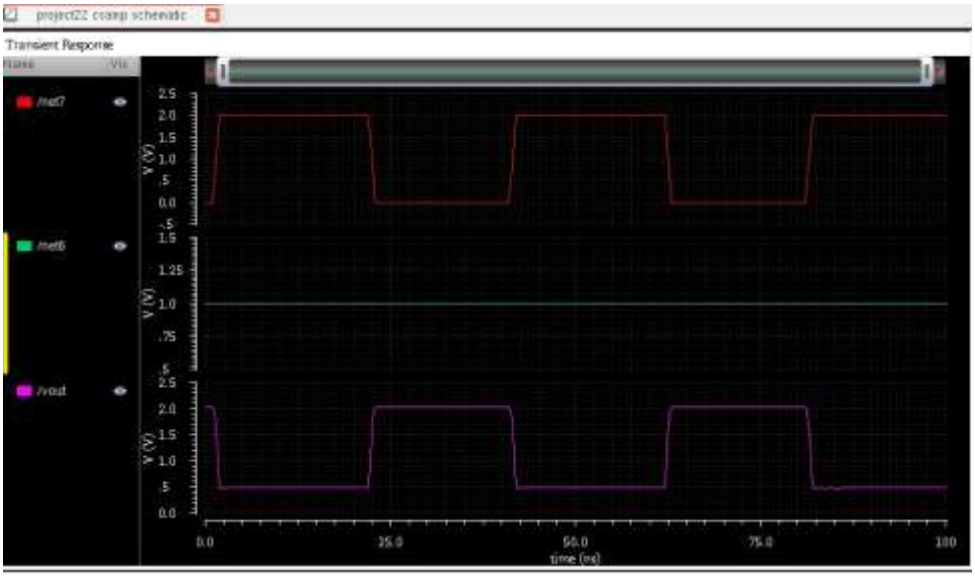

Figure: 7 Common Source output

c. OP-Amplifier

Figure: 8Op-Amplifier output

Performance Summary

Parameters	Constraint values (Outputs)
Node	90nm
Resolution bits	12

Supply voltage	1.8 V
Power Consumption(mW)	25
Area	0.054mm^2
Gain	55dB

Conclusion

A two-stage OP-AMP is designed with a DAC with R-2R ladder resistor to achieve high gain. The DAC is designed and its various characteristics are measured. Cadence 90nm technology is used in this simulation to simulate a DAC with a gain of 55dB and consumption of 25mW. It is less efficient than 180nm technology as the supply voltage is less.

Future Scope

This work can be upgraded with increasing the no of bits , increasing gain. Lower technology nodes will give better result in terms of power, area and gain.

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