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Design metrics for operational tran conductance amplifier

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***Abstract*---**It is a highly tough undertaking to build an analogue circuit, especially one that consumes little power [1-5]. A basic component in many analogue integrated circuits like ADC, Gm-C filter and Delta Sigma modulator is the Operational Transcondactance Amplifier commonly known as the OTA. In all of these integrated circuits, the structure of the OTA is of fundamental importance. Gain Bandwidth (GBW), DC Gain, Common Mode Rejection Ratio (CMRR) and average power are performance characteristics that decide the selection of the OTA [6]. A well-designed OTA that has outstanding processing attributes such as speed, power consumption, gain and GBW is an accomplishment in itself [15]. This chapter mainly examines the performance parameters theoretically as well as analytically, which determines the design of OTA. Optimization strategies which are applicable to low voltage and low power applications, notably at the level of the transistor are also examined.

***Keywords*---**OTA Construction, Transcondactance Amplifier, OTA Telescope.

Introduction

The OTA architecture that is employed must be application-specific and must ensure enough performance within the power and area constraints [20, 25]. Three essential OTA structures are addressed in detail in Figure 3.1: Telescopic, Folded Cascode (FC), and Recycling Folded Cascode (RFC) OTAs. The next sections explore the aforementioned topologies in detail with regard to their performance metrics;

(a) OTA Telescopic:

The Telescopic OTA provides the best frequency response and is also the most energy efficient structure. It is also a structure that reflects the least amount of

noise. Despite these advantages, it is the least suitable for low voltage applications since it provides the least headroom for signal swing at the output and requires more power than the Folded Cascode OTAs. Taking everything into perspective, the Telescopic OTA is the best solution for systems requiring extremely high speed and low noise performance, as well as for designs where signal swing is not a key factor [29-36].

(b) Folded Cascode (FC) OTA:

Due to the fact that this OTA shares the advantage of a good frequency performance with the Telescopic OTA, albeit at a reduced efficiency, and also shares the advantage of a decent low voltage performance without additional noise with the Current Mirror OTA [30 - 33], it serves as an excellent middle ground OTA.

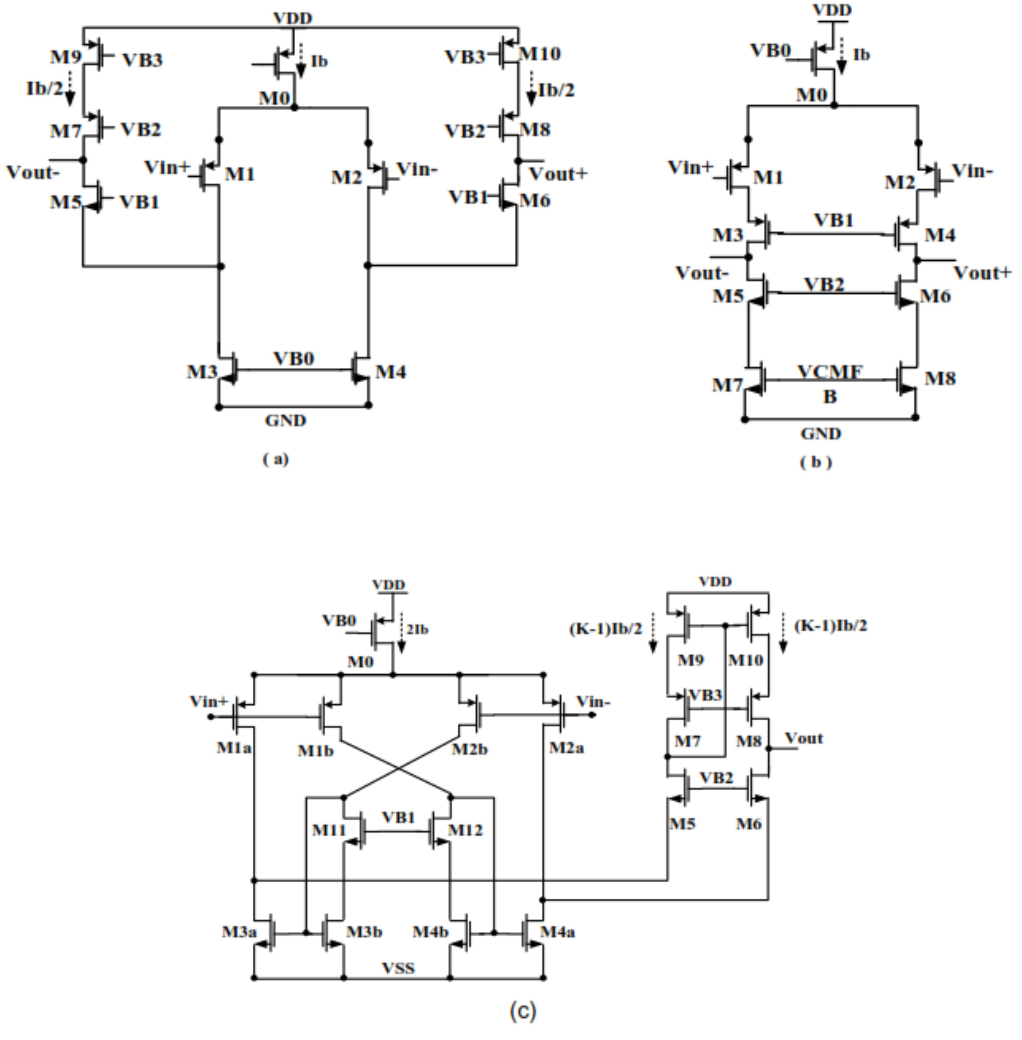

Figure 3.1. (a) Folded cascode OTA (b) Telescopic OTA (c) Recycling Folded Cascode OTA

The Folded Cascode OTA is best suited for applications where speed, signal headroom, and noise are critical. As a result, it's unsurprising to see the Folded Cascode amplifier being utilised more frequently as a single stage or as the first stage amplifier in multi-stage amplifiers, both in cutting-edge designs and in the literature.

(c) Recycling Folded Cascode (RFC) OTA:

Is illustrated in Figure 3.1 (c) with the PMOS input stage. Its development requires that the current sources are modified at the folding stage using active current mirrors with a current ratio of 1:K and then reconnected to differential pair transistors. It is worth noting that the power consumption is identical to that of the FC OTA when K=3. The transistors M11-M12 improve the accuracy and stability of current mirrors. This approach boosts the OTA's transconductance, GBW, and SR without increasing current consumption, as folding is accomplished using active current mirrors with a current gain K that scale the differential pair's signal currents.

Numerous design considerations for Telescopic, FC, and RFC OTAs will be explored in the following sections. To simplify this discussion, we will frequently refer to the square law I-V model of MOS devices under saturation. The equation used to express this is (3.1). N, Cox, W, L, VGS, VT, and VGST are the electron mobility, gate oxide per unit area, width, length, gate-source, threshold, and overdrive voltages, respectively, in this equation.

$$I_{D0} = \frac{1}{2}\mu_N C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 = \frac{1}{2}\mu_N C_{ox}\frac{W}{L}V_{GST}^2 \qquad (3.1)$$

While this model does not account for many second order effects that are inherent in and serve as a model for cutting-edge CMOS technology, its performance is a near approximation to that of a MOS device. However, if necessary and pertinent, secondary order effects will be demonstrated.

Effective Transconductance:

Transconductance, or gm, is the capacity of the OTA to transform the input voltage signal to a current that drives the output load [6]. It is expressed as follows:

$$G_m = \frac{I_{out}}{V_{GS}}$$

By and large, the OTA's effective transconductance equals the input stage's transconductance. As a result of the symmetry of the construction, the transconductance of the Telescopic and FC OTAs is represented as,

$$G_{mTL} = gm_{1,2} = G_{mFC} \quad (3.2)$$

In case of RFC OTA,

$I_{out} = g_{m1a}V_{in+} + g_{m3a}V_{in-}$

From Figure 3.1., $V_{in+} = V_{in-}$ and $g_{m3a} = Kg_{m1a}$. This adjustment causes an output current as

$I_{out} = g_{m1a}V_{in+} + Kg_{m1a}V_{in+}$

$I_{out} = (1 + K)\, g_{m1a}\, V_{in+}$

So, the effective transconductance of RFC OTA will be,

$$G_{mRFC} = (1 + K)g_{m1a} \quad (3.3)$$

For factor K = 3, the G_{mRFC} shows 100% improvement over G_{mFC} where G_{mFC} is the transconductance of FC OTA. As the M1 in the FC OTA is double the size of M1a and conducts two times the current for the same biasing voltages,

$G_{mFC} = 2g_{m1a} = G_{mTL}$

Small Signal Bandwidth:

The speed performance of an amplifier is the major indicator of its bandwidth. Additionally, it represents the frequency range across which the amplifier's gain is greater than unity, and is sometimes referred to as the gain bandwidth product (GBW). The quiescent operating point, the device size, the CMOS technology used, the amplifier architecture, and the driven load are only a few of the numerous variables that affect an amplifier's GBW. To incorporate more gates per unit area, CMOS technology has aggressively scaled down its device size over the last four decades. The bandwidth has increased as a result of this downsizing. The transit frequency, f T, is the most frequently used Figure of Merit (FoM) for determining the maximum speed achievable with any CMOS technology. This is the point at which the MOS device's small signal drain current to gate current ratio equals one. Equation (3.4) states that the speed of CMOS devices, and hence the speed of a CMOS amplifier, can be increased by increasing the overdrive voltage, V_{GST}, or by decreasing the device channel length, L.

$$f_T \cong \frac{\mu}{2\pi}\frac{V_{GST}}{L^2} \quad (3.4)$$

However, from a designer's perspective, what determines an amplifier's bandwidth, and thus its speed, is the transconductance and load of the amplifier. The GBW can be represented as follows for Telescopic, FC, and RFC amplifiers:

$$GBW_{RFC} \cong \frac{G_{mRFC}}{C_L} = \frac{(K+1)g_{m1a}}{C_L}$$

$$GBW_{TL} \cong GBW_{FC} = \frac{2g_{m1a}}{C_L}$$

Where C_L is the capacitance of the load. For K=3, the RFC OTA outperforms the Telescopic and FC OTAs by a factor of 100.

Gain at low frequency:

The low frequency gain of a CMOS amplifier is the product of its effective transconductance and intrinsic output resistance [29-33]. According to (3.3), the effective transconductance of the RFC OTA is twice that of the FC and Telescopic OTAs when the supply voltage and biassing current are identical. Additionally, for FC and RFC OTA, the inherent output resistance can be stated as,

$$R_{oRFC} = g_{m6}r_{o6}(r_{o2a}||r_{04a})||g_{m8}r_{08}r_{010}$$

$$R_{oFC} = g_{m6}r_{o6}(r_{o2}||r_{04})||g_{m8}r_{08}r_{010}$$

$$R_{oTL} = g_{m3}r_{o1}r_{o3}||g_{m5}r_{05}r_{07}$$

It has been demonstrated that $G_{mRFC} = 2G_{mFC}$, resulting in a gain enhancement of around 6-7dB for the same output impedance. Nonetheless, R_{oRFC} outperforms R_{oFC} because transistors M_{2a} and M_{4a} conduct less current than their FC equivalents M2 and M_4. This increases their intrinsic output impedance, r 0, as a result. The increase in r o2a and r o4a enables an extra 2-4dB gain boost in the RFC. Thus, when compared to the FC and Telescopic OTA, the RFC can achieve an overall gain enhancement of 8-10dB at low frequencies. As a result, settling errors associated with finite amplifier gain are reduced when an RFC is used instead of an FC [42].

Phase Margin:

The phase margin is a measure of the amplifier's stability and is measured at s=GBW. It also indicates the ability of an amplifier to attain a steady state with the application of a fast time varying signal like step signal at its input terminal [28]. The cumulative effect of the poles and zeros provides the phase [29]. Equation (3.7) gives the general phase expression for a transfer function with n poles (ω_p) and m zeros (ω_z).

$$\emptyset(\omega) = \sum_{l=1}^{n} \tan^{-1}\left(\frac{\omega}{\omega_{pl}}\right) - \sum_{k=1}^{m} \tan^{-1}\left(\frac{\omega}{\omega_{zk}}\right) \quad (3.7)$$

The phase margin can be intuitively analyzed as follows. Normally, the magnitude of the amplifier transfer function is the decreasing order of function s. If phase shift between V_{out} and V_{in} exceeds 180° at some frequency ω_o while the amplifier's gain is greater than unity (ω_o< GBW), for some transfer function with multiple poles, then the amplifier's output will oscillate indefinitely and become unstable. Generally, the ideal phase margin for high speed performance is around 60° [32]. This is indeed the case for the chosen settling error (0.1%).

The RFC has the same poles as FC. But it also has an additional pole-zero pair, ω_{p2} and ω_{z1}, which is associated with the current mirrors M3a:M3b (and M4a:M4b). Nevertheless, this pole-zero pair is also associated with NMOS devices, and this puts it at a high frequency [42]. Equation (3.8) shows the expected phase margin expression. Equation (3.9) shows the corresponding pole-zero locations.

$$PM_{RFC} = 180^0 - tan^{-1}\left(\frac{\omega_u}{\omega_{p1}}\right) - tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right) - tan^{-1}\left(\frac{\omega_u}{\omega_{p3}}\right) + tan^{-1}\left(\frac{\omega_u}{\omega_{z1}}\right) \quad (3.8)$$

$$\omega_u = \frac{G_{mRFC}}{C_L}, \omega_{p1} = \frac{-1}{R_{oRFC}C_L}, \omega_{p2} \cong \frac{-g_{mb3}}{(K+1)C_{gs3b}}, \omega_{p3} \cong \frac{-g_{m5}}{C_{gs5}}, \omega_{z1} \cong (K+1)\omega_{p2} \quad (3.9)$$

The selection of factor K is a major factor in the determination of the phase margin, so the choice of K will be restricted by the application of the amplifier; in case of applications that are high speed, ideally, K is chosen such that ω_{p2}> 3ω_u, which can be utilized to put an upper boundary on K. This is shown by Equation (3.10).

$$\omega_{p2} > 3\omega_u \rightarrow K < \sqrt{\frac{g_{mb3}C_L}{3g_{m1a}C_{gs3b}}} - 1 \quad (3.10)$$

Similarly, phase margin for Telescopic and FC OTAs are given in (3.11) and (3.12) respectively.

$$PM_{TL} = 180^0 - tan^{-1}\left(\frac{\omega_u}{\omega_{p1}}\right) - tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right) \quad (3.11)$$

$$\omega_u = \frac{gm_1}{C_L}, \omega_{p1} = \frac{1}{R_{oTL}C_L}, \omega_{p2} \cong \frac{g_{m3}}{C_{gs3}}$$

$$PM_{FC} = 180^0 - tan^{-1}\left(\frac{\omega_u}{\omega_{p1}}\right) - tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right) \quad (3.12)$$

$$\omega_u = \frac{gm_1}{C_L}, \omega_{p1} = \frac{1}{R_{oFC}C_L}, \omega_{p2} \cong \frac{g_{m5}}{C_{gs5}}$$

In comparison to the Telescopic and FC structures, the RFC OTA has a somewhat narrower phase margin because to the additional pole introduced by recycling the current mirror.

Slew Rate:

To achieve a minimally acceptable linearity in applications such as switch capacitors, precision and setting time are critical characteristics. The maximum output current imposes a restriction on the amount of time an amplifier may settle [37]. The current utilised to bias the amplifier imposes a limit on the amplifier's ability to drive current into its output impedance [87]. In Figure 3.1, transistor M_0, which serves as the OTA's tail, supplies the OTA with the biassing current I_b.

When Vin+ is high, the input state transistors M1a and M1b switch off, which induces the current mirror transistors M4a and M4b into an off state. As a result, M2a is changed to a deep triode configuration, while M4a's drain potential increases and M6 is turned off. This directs the tail current, Ib, into M2b, which is mirrored into M5 by a factor of K (M3b:M3a). As a result, the total current required to discharge CL at Vout- is Ib(3K+1)/4. At Vout+, however, only Ib(K 1)/4 is available to charge CL. This results in a common mode error. The common mode feedback compensates for this inaccuracy by ensuring that the current discharging/charging CL at each output is same and equal to Klb/2. When Vin- levels rise, a reversal of events occurs. As a result, the slew rate is symmetric and can be stated mathematically using equation (3.13) for a differential load of CL/2. The FC and Telescopic OTA slew rates are repeated in equation (3.14)

$$SR_{RFC} = \frac{KI_b}{C_L} \tag{3.13}$$

$$SR_{FC} = SR_{TL} = \frac{I_b}{C_L} \tag{3.14}$$

When K=3, the RFC's slew rate increases by a factor of three when compared to the FC and Telescopic OTAs, while its power consumption remains constant. Devices that are assumed to turn off completely yet nevertheless conduct some residual current, so lowering the amount of current reaching the output. Additionally, there is a decrease in the accuracy of the current mirrors during large transients. However, with proper device size and biassing, it is possible to achieve a more than 2-fold increase in slew rate when K=3 [28].

Noise:

As a general rule, noise in circuits is described as spontaneous variations in current, temperature, or voltage that establish the lower limit for measurements conducted on a system under test. These oscillations limit the dynamic performance of a system in a variety of applications, including continuous time filters, audio amplifiers, and data converters [39].

Thermal and flicker noise are the two major forms of noise that impair the performance of CMOS circuits [28, 41, 42]. Thermal noise is caused by random charge carrier mobility in a conductor caused by the ambient temperature. The interaction of the Si-SiO2 interface with the charge carriers is a significant source

of flicker noise. In this situation, the carriers are caught and subsequently released back into the channel as a result of a random process. It is feasible to model these noise sources in MOS devices by connecting them to the device that depicts the power spectral density as a current source. This is expressed mathematically (3.15). The first and second terms denote the thermal and flicker noise contributions, respectively. Boltzman's constant, absolute temperature, noise factor, process-dependent flicker noise coefficient, and frequency are denoted by the symbols k, B, T,, K F, and f.

$$\overline{i_o^2} = \left(4k_B T\gamma g_m + \frac{K_F I_D}{C_{ox} L^2 f}\right)\Delta f \qquad (3.15)$$

The proposed changes in the RFC contain more devices and alter the signal's route. As a result, it is critical to investigate their effects on the performance of noise. The thermal and flicker noise components of the RFC are examined separately in order to compare them to the FC. Equation (3.16) can be used to represent the greatest noise seen at the output as,

$$\overline{i_o^2} = \overline{i_{1a}^2} + \overline{i_{1b}^2} + \overline{i_{3a}^2} + \overline{i_{3b}^2} + \overline{i_9^2} \qquad (3.16)$$

Equation (3.16) initiates the examination of the RFC's output current thermal noise PSD. The cascade devices are not included in Equation (3.17).

$$\overline{i_{oT}^2} = 4K_B T\gamma[2g_{m1a} + 2K^2 g_{m1b} + 2g_{m3a} + 2K^2 g_{m1b} + 2g_{m9}] \qquad (3.17)$$

In RFC OTA, $g_{m1a} = g_{m1b}$ and $g_{m3a} = K.g_{m3b}$, (3.18) becomes

$$\overline{i_{oT}^2} = 8K_B T\gamma[(1+K^2)\, g_{m1a} + (1+K)g_{m3a} + g_{m9}] \qquad (3.18)$$

The result obtained from (3.18) can be referred to the input through the transconductance, G_{mRFC}, of the amplifier as expressed in (3.19). This results in the input referred thermal noise spectral density.

$$\overline{V_{iT}^2} = \frac{\overline{i_{oT}^2}}{G_{mRFC}^2} = \frac{8K_B T\gamma}{(1+K)g_{m1a}}\left[\frac{(1+K^2)}{(1+K)} + \frac{g_{m3a}}{g_{m1a}} + \frac{g_{m9}}{(1+K)g_{m1a}}\right] \qquad (3.19)$$

By maximizing $(W/L)_{1a}$ and minimizing $(W/L)_{3a}$, $(W/L)_9$ and K it is possible to minimize the thermal noise component. It is however, essential that K must be greater than 1, else M5-M10 will conduct zero current. Evaluation of input referred flicker noise spectral density can similarly be done as,

$$\overline{V_{if}^2} = \frac{K_{FP}}{\mu_p C_{ox}^2 W_{1a} L_{1a} f}\left[\frac{(1+K^2)}{(1+K)^2} + \frac{K}{(1+K)}\frac{K_{FN}}{K_{FP}}\left(\frac{L_{1a}}{L_{3a}}\right)^2 + \frac{(K-1)}{(1+K)^2}\left(\frac{L_{1a}}{L_9}\right)^2\right] \quad (3.20)$$

We can maximize W_{1a}, L_{3a} and L_9 and minimize K in order to minimize the flicker noise component. Equations (3.21) and (3.22) express the input referred thermal noise spectral density for Telescopic and FC structures respectively.

$$\overline{V_{iT,TL}^2} = \frac{\overline{i_{oT}^2}}{G_{mTL}^2} = \frac{8K_B T\gamma}{g_{m1}}\left[1 + \frac{g_{m3}}{g_{m1}}\right] \quad (3.21)$$

$$\overline{V_{iT,FC}^2} = \frac{\overline{i_{oT}^2}}{G_{mFC}^2} = \frac{8K_B T\gamma}{g_{m1}}\left[1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}}\right] \quad (3.22)$$

Due to the fact that transistor gates in CMOS technologies are typically n+polysilicon, PMOS devices exhibit buried-channel behaviour. This reduces the interface's interaction with the carriers and hence the flicker noise coefficient [28, 39, 43]. As a result, K FP is an order of magnitude smaller than K FN. As a result, PMOS devices are well-suited for use as input pair devices to minimise flicker noise. K FP and K FN, on the other hand, are of the same order for p+ polysilicon gates. Nonetheless, given advancements in CMOS technology, the contribution of each type of noise varies. As seen in Equation (3.15), flicker noise is inversely proportional to frequency, whereas thermal noise has a flat frequency dependence. In general, when all factors are considered, it is preferable to use PMOS devices as the input pair of amplifiers.

To summarise, the following guidelines can be followed to enhance amplifier noise performance for low voltage, low power, and high-speed applications:

- If p+ polysilicon is not used for the gate material or if the aims are particularly high-speed applications (GHz range), it is preferable to employ PMOS devices for the input pair.
- The I_D of the input pair should be maximised within the constraints of the specified power budget.
- The input pair devices' area and aspect ratio (WL and W/L) should be optimised.

Offset of the Input:

The primary source of device incompatibilities throughout the chip is manufacturing process variance. To analyse the MOS transistor mismatch, the drain current mismatch is the essential factor to examine. The effect of process variation on the variance of MOS drain current is illustrated in [40] and is represented as,

$$\sigma^2(I_D) = 4I_D^2 \frac{\sigma^2(V_T)}{(V_{GS}-V_T)} + I_D^2 \frac{\sigma^2(\beta)}{\beta^2}$$

Here V_{GS}, V_T and β amount to gate to source voltage, threshold voltage and μCox (W/L) of the MOS transistor. In the same way, variance in V_{GS} is expressed as,

$$\sigma^2(V_{GS}) = \sigma^2(V_T) + \frac{I_D^2}{g_m^2}\frac{\sigma^2(\beta)}{\beta^2} \quad (3.23)$$

Since (g_m/I_D) is generally maximum for analog design, the impact of the second term in (3.23) can be ignored because (g_m/I_D) is generally maximum for analog design. Hence,

$$\sigma^2(V_{GS}) = \sigma^2(V_T) = \frac{A_{V_T}^2}{WL}$$

where, A_{V_T} represents the threshold voltage area which is proportionality constant. An effective drain current variance for RFC OTA is expressed as,

$$\sigma^2(I_D) = 2\left[A_{VTP}^2\left(\frac{g_{m1a}^2}{W_{1a}L_{1a}} + K^2\frac{g_{m1b}^2}{W_{1b}L_{1b}}\right) + A_{VTN}^2\left(\frac{g_{m3a}^2}{W_{3a}L_{3a}} + K^2\frac{g_{m3b}^2}{W_{3b}L_{3b}}\right) + A_{VTP}^2\frac{g_{m9}^2}{W_9L_9}\right]$$

In RFC, $W_{1a} = W_{1b}$, $L_{1a} = L_{1b}$, $W_{3a} = KW_{3b}$, $L_{3a} = L_{3b}$, $g_{m1a} = g_{m1b}$, and $g_{m3a} = Kg_{m3b}$.

$$\sigma^2(I_D) = 2\left[A_{VTP}^2\left(\frac{g_{m1a}^2}{W_{1a}L_{1a}}(1+K^2)\right) + A_{VTN}^2\left(\frac{g_{m3a}^2}{W_{3a}L_{3a}}(1+K)\right) + A_{VTP}^2\frac{g_{m9}^2}{W_9L_9}\right] \quad (3.24)$$

Through G_{mRFC}, it is possible to convert the result in Equation (3.24) to the input referred offset. After some algebra this results in the input offset variance as:

$$\sigma^2(V_{OS,RFC}) = 2\left(\frac{A_{VTP}^2}{W_{1a}L_{1a}}\right)\left[\frac{(1+K^2)}{(1+K)^2} + \frac{K}{(1+K)}\frac{\mu_N}{\mu_P}\left(\frac{A_{VTN}}{A_{VTP}}\right)^2\left(\frac{L_{1a}}{L_{3a}}\right)^2 + \frac{(K-1)}{(1+K)^2}\left(\frac{L_{1a}}{L_9}\right)^2\right] \quad (3.25)$$

We can maximize W_{1a}, L_{3a} and L_9, and minimize K in order to minimize the input offset. Equations (3.26) and (3.27) express the input offset variance for the Telescopic and FC OTA respectively.

$$\sigma^2(V_{OS,TL}) = 2\left(\frac{A_{VTP}^2}{W_1L_1}\right)\left[1 + \frac{\mu_N}{\mu_P}\left(\frac{A_{VTN}}{A_{VTP}}\right)^2\left(\frac{L_1}{L_7}\right)^2\right] \quad (3.26)$$

$$\sigma^2(V_{OS,FC}) = 2\left(\frac{A_{VTP}^2}{W_1L_1}\right)\left[1 + 2\frac{\mu_N}{\mu_P}\left(\frac{A_{VTN}}{A_{VTP}}\right)^2\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_9}\right)^2\right] \quad (3.27)$$

As a result of the scaling down of CMOS technologies in terms of tox, a decrease in A_{VT} resulting in an improvement in the matching hcaracteristics. However, because the device's dimensions are reduced as well, this is not fully reflected in the device matching, resulting in a reduction in matching performance. However, the dependence on the doping dose in the bulk is an interesting element to consider. Low V_T devices are becoming more robust as a result of advancements in CMOS technology, and their applications in low voltage applications are growing more diverse. The reduction in V_T is due to a counter type implant in the

bulk region just below the gate where the channel is established. This significantly reduces the total dose while improving their matching performance when compared to conventional devices.

Efficiency:

Efficiency, η, in the case of an amplifier is defined as the ratio of the amplifier transconductance to the quiescent DC current consumed [28]. Given below is the efficiency of the Telescopic, FC and RFC OTAs, which is expressed as,

$$\eta_{TL} = \frac{G_{mTL}}{I_{Total}} = \frac{g_{m1,2}}{I_b}$$

$$\eta_{FC} = \frac{G_{mFC}}{I_{Total}} = \frac{g_{m1,2}}{2I_b}$$

$$\eta_{RFC} = \frac{G_{mRFC}}{I_{Total}} = \frac{2g_{m1a}}{I_b}$$

The RFC's efficiency is double that of the FC and is comparable to that of the Telescopic OTA. More importantly, the RFC's efficiency is independent of the present mirror factor K.

Conclusion

The following is a list of some critical elements that must be considered during the selection and design of an OTA, based on the theoretical and analytical discussion:

- Despite the fact that each application requires a unique amplifier design, the most critical parameters in the design are the amplifier's bandwidth, gain, and slew rate.
- The research above demonstrates unequivocally that the RFC delivers two times the bandwidth, an estimated gain of 810dB, and a slew rate more than twice that of the FC and Telescopic OTAs for a nearly equal area and power consumption.
- Additionally, the RFC OTA requires half the power of the Telescopic and FC OTAs while providing comparable performance. It is best suited for applications requiring low voltage and low power.

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